ABSTRACT OF THE DISCLOSURE

A multiplexer cell layout structure is a layout structure of primitive cells where cell arrays composed of P-channel transistors and N-channel transistors are arranged in two upper and lower rows. And, a plurality of transistors of transfer gates are arranged on the upper side and lower side of the cell arrays, an output terminal of the plurality of arranged transistors is connected up and down by Metal wiring across between the upper and lower cell arrays. Thus, a multiplexer cell layout structure which increases wiring tracks of two-layer metal wiring for a one-chip layout held by a 4-input multiplexer inverter can be obtained.